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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,583	04/22/2004	Hsuch-Chung Chen	252011-2240	6746

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,583	CHEN ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 22-25* is/are rejected.

7)☒ Claim(s) *13-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 3-6, 8-12 and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Kunikiyo (US 6,717,267).

2. Regarding claims 1 and 23, Kunikiyo (e.g. fig. 8) shows a semiconductor configuration for dissipating heat away from a semiconductor device having a plurality of power bus lines, comprising: a semiconductor substrate 1, and a plurality of interconnect structures (26c, 25a, 26a, 21a,c, 22a, 9a) disposed on the substrate and in contact therewith and extending through the semiconductor device, the interconnect structures for dissipating heat through the substrate (col. 9/lls. 1-6). Note that the heat flow from the active device in the substrate to the non-active area and then to the dummy patterns.

3. Regarding claim 3, Kunikiyo shows that the each of the plurality of interconnects structures comprises at least one via stack 9a.

4. Regarding claim 4, Kunikiyo shows that the plurality of interconnects structures are close to a power line 19c (see fig. 13).

5. Regarding claim 5, Kunikiyo shows that at least one of the plurality of interconnect structure (26a, 26c) is joined to one other of the plurality of interconnect structures using a bridge structure 25a..

6. Regarding claim 6, Kunikiyo shows bridge structures 25a, each of the bridge structures joins a respective one of the plurality of interconnect structures (26a, 26c)

7. to one other of the plurality of interconnect structures.

8. Regarding claim 8, Kunikiyo shows that the interconnect structures (26c, 26a) are spaced apart form each other by width of one of the interconnect structures (e.g. 25a).

9. Regarding claim 9, Kunikiyo shows that the plurality of interconnect structure (26c and 26a) is alternatively spaced apart form a serpentine power line 25a by a distance (e.g. fig. 9).

10. Regarding claim 10, Kunikiyo shows that the distance is a width of one of the plurality of interconnect structures (e.g. 25a).

11. Regarding claim 11, Kunikiyo shows that each of the interconnect structures (21c) is spaced apart from a power line 19c by a distance (see fig. 13).

12. Regarding claim 12, Kunikiyo shows that the distance is the width of one of the plurality of interconnect structures (e.g. 21a).

13. Regarding claim 22, Kunikiyo (e.g. fig. 8) shows a semiconductor configuration for dissipating heat away from a semiconductor device having a plurality of power bus lines, comprising: a semiconductor substrate 1; and a plurality of interconnect structures (26c, 25a, 26a, 21a,c, 22a, 9a), each of the interconnect structures having at least one

via stack, the interconnect structure disposed on the substrate and in contact therewith and extending through the semiconductor device, the interconnect structures for dissipating heat through the substrate (col. 9/lls. 1-6). Note that the heat flow from the active device in the substrate to the non-active region and then to the dummy patterns.

14. Regarding claim 24, Kunikiyo (e.g. fig. 8) shows a method for forming a semiconductor configuration for dissipating heat away from a semiconductor device having a plurality of power bus lines, comprising: providing a semiconductor substrate 1, and a forming plurality of interconnect structures (26c, 25a, 26a, 21a,c, 22a, 9a) disposed on the substrate and in contact therewith and extending through the semiconductor device, the interconnect structures for dissipating heat through the substrate (col. 9/lls. 1-6). Note that the heat flow from the active device in the substrate to the non-active region and then to the dummy patterns.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

17. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kunikiyo (US 6,717,267).

18. Regarding claim 7, Kunikiyo teaches most aspects of the instant invention including an interconnection structure having a width (i.e.. design variable col. 15/lls. 24-41), but does not disclose that the interconnect structure is from about 0.1 to 10 micrometers. Nonetheless, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Also, the specific width claimed by applicant, i.e., from about 0.1 to 10 micrometers, absent any criticality, is only considered to an optimum value of the interconnect width structure disclosed by the Prior Art that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of the prior art, will be obtained as long as an interconnect structure is used as already suggested by the Prior Art.

19. Claims 2 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunikiyo (US 6,717,267) in view of Khan et al. (US 6,853,070).

20. Regarding claims 2 and 25, Kunikiyo shows most aspects of the instant invention including a substrate but does not disclose a heat sink in contact with the substrate. Nevertheless, Khan (e.g. fig. 2A) shows a mounting structure including a heat sink 110/134 in contact with the substrate 102. According to Kahn this type of mounting structure provides an improved thermal, mechanical and electrical performance because the thermal stress is reduced due to a matched thermal coefficient (col. 1/lls. 52-67; col. 2/lls. 1-6 and col. 3/lls. 14-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the device disclosed by Kunikiyo in the mounting structure disclosed by Khan which includes a heat sink in contact with the substrate to provide a semiconductor package having a reduce thermal stress in order to improve the thermal, mechanical and electrical performance of the package.

Allowable Subject Matter

21. Claims 13-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-

1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Andújar
Patent Examiner
Art Unit 2826
08/08/2005